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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,386	07/23/2003	Sundeep Chauhan	STL10986	2363

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EXAMINER	
NGUYEN, HAI L	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 11/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,386	CHAUHAN, SUNDEEP	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7-12,16-22,25 and 26* is/are rejected.

7)☒ Claim(s) *4-6,13-15,23 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Appeal Brief

1. Applicant's appeal brief filed on 6/28/2006 has been received and entered in the case. The prior art rejection, mailed on 2/15/2006, has been withdrawn because the prior Office Action has not fully address all the issues. Applicant's arguments with respect to the prior art rejection, mailed on 2/15/2006, have been fully considered but are not deemed to be persuasive. A new action on the merits appears below.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 7, 10-12, 16, 17, 20-22, 25, 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Staszewski et al. (US Pat. 6,429,693; previously cited).

With regard to claim 1, Staszewski et al. discloses in Figs. 1-8 an apparatus comprising a phase/frequency comparator circuit (200) that is configured to generate a phase error (202) responsive to a transition location signal (TDC_RISE, TDC_FALL; as discussed in the prior office action mailed on 02/15/2006)

With regard to claim 7, the phase/frequency comparator further comprises a phase detecting stage that generates a result (Q(0)-Q(L-1)) that represents an instantaneous phase

difference; and encoding circuitry (NORM) coupled to the phase detecting stage; wherein the encoding circuitry converts a result of the phase detecting stage into a numerical phase difference value (PHF).

With regard to claim 2, the phase detecting stage further comprises a tapped delay line (502s) having a plurality of outputs and configured to receive a first signal (CKV); and a parallel latch coupled to the plurality of outputs of the tapped delay line and configured to receive a second signal (110), wherein the parallel latch stores the values of the plurality of outputs of the tapped delay line in response to a transition in the second signal; and wherein the encoding circuitry converts the values stored in the parallel latch into a numerical phase difference value.

With regard to claim 3, the phase/frequency comparator further comprises an accumulator (102) coupled to the encoding circuitry, wherein the accumulator adds the numerical phase difference value to a value stored in the accumulator to obtain an accumulated phase error (PHE).

With regard to claim 10, Staszewski et al. discloses in Figs. 1-8 a phase locked loop comprising a controllable oscillator (103); and a phase/frequency comparator includes a phase detecting stage (201); encoding circuitry (NORM) coupled to the phase detecting stage; and an accumulator (102) coupled to the encoding circuitry.

With regard to claim 11, the phase detecting stage further comprises a tapped delay line (502s) having a plurality of outputs and configured to receive a first signal (CKV); and a parallel latch coupled to the plurality of outputs of the tapped delay line and configured to receive a second signal (110), wherein the parallel latch stores the values of the plurality of outputs of the tapped delay line in response to a transition in the second signal; and wherein the encoding

circuitry converts the values stored in the parallel latch into a numerical phase difference value (PHF).

Claim 12 is similarly rejected; note the above discussion with regard to claim 3.

With regard to claim 16, the forward path includes additional control circuitry (105).

With regard to claim 17, the reference also meets the recited limitation in the claim.

With regard to claim 20, Staszewski et al. discloses in Figs. 1-8 a corresponding method comprising the steps of generating a snapshot (Q(0)-Q(L-1)) of a first signal (114) in response to receiving a second signal (110); and mapping the snapshot to a numerical phase difference value (PHF) that is generated responsive to a signal that corresponds to a transition location of the first signal (TDC_RISE, TDC_FALL).

With regard to claim 21, the method further comprises the steps of combining the numerical phase difference value (PHF) with a value in an accumulator (102) to obtain a new accumulator value; and presenting the new accumulator value (PHE) as a result of a phase comparison.

With regard to claim 22, the method further comprises the steps of propagating the first signal (114) through a tapped delay line (502s); latching outputs of the tapped delay line in a parallel latch (504s) in response to a transition in the second signal (110) to obtain the snapshot of the fist signal.

With regard to claims 25 and 26, controlling an output frequency (RF OUT) of an oscillator (103) using the result of the phase comparison, wherein the first signal (CKV) is an output of the oscillator (RF OUT through 106).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 8 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Staszewski et al. in view of Brachmann et al. (US 6,351,154; previously cited).

With regard to claim 8, the above discussed the apparatus of Staszewski et al. meets all of the claimed limitations except that Staszewski et al. does not disclose the apparatus is implemented on a single monolithic integrated circuit. Brachmann et al. teaches in Fig.5 a similar apparatus can be implemented as integrated circuit (column 4, lines 20-33) as recited in the claim. Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to implement that teaching with the apparatus of Brachmann et al. for the advantage of reducing additional cost when implemented within other circuits, e.g. ASIC, PLD, FPGA, PLL etc.

Claim 18 is rejected for similar motivation; note the above discussion with regard to claim 8.

6. Claims 9 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Staszewski et al.

With regard to claims 9 and 19, the above discussed circuit of Staszewski et al. meets all of the claimed limitations except for the intended use as implemented in a field programmable gate array. However, it is noted that the reference circuit has the ability to be used in this

environment as well. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to implement that circuit taught by Staszewski et al. in the field programmable gate array for the advantage of saving power consumption from the circuit.

Response to Arguments

7. Applicant has repeatedly argued that the claimed *transition location signal* has the following meaning (as disclosed in the specification; page 7, lines 1-10):

> N-bit parallel latch 302 latches in the outputs of N-bit tapped delay line 300 when reference clock signal 303 transitions (either from low to high or high to low, depending on the latch design). The output of N-bit parallel latch 302 is thus a snapshot of the progress of input signal 301 through N-bit tapped delay line 300 over one cycle of reference clock signal 303. This snapshot is fed into N-bit edge detect circuit 304, which is described in more detail in FIG. 4. N-bit edge detect circuit 304 outputs a single bit at the transition point of a falling edge (or rising edge, depending on the design) in the snapshot provided by N-bit parallel latch 302. This signal bit may be referred to as a transition location signal.

Applicant has repeatedly argued that "This signal bit may be referred to as a transition location signal." (Emphasis added) is considered as a clear definition. However, Examiner respectfully disagree because that statement is seen as an example, which describes the operation of the invention rather than as a special definition. There is no special definition which specifies the term *transition location signal* is found in the specification. In order to be recognized as specific definition, a special definition paragraph for defining a specific term must be provided in the specification. Unless otherwise defined, the claimed term "*transition location signal*" should be interpreted in light of the ordinary and customary meaning as understood by those skilled in

the art. This means that the words of the claim must be given their plain meaning unless applicant has provided a special definition for a specific term in the specification. In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989); Chef America, Inc. v. Lamb-Weston, Inc., 358 F.3d 1371, 1372, 69 USPQ2d 1857 (Fed. Cir. 2004).

As discussed above, the term "*encoding circuitry*" should be interpreted in light of the ordinary and customary meaning as understood by those skilled in the art. Unless otherwise defined with a special definition for that term.

Allowable Subject Matter

8. Claims 4-6, 13-15, 23, and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose or fairly suggest a phase/frequency comparator (as shown in Fig. 3), and a method of use thereof, as recited in claims 4, 13, and 23, having specific structural limitations such as an encoding circuitry includes an edge detector (304) coupled to the parallel latch (300, 302); and a weighted encoder (306), wherein the edge detector outputs a transition location signal that indicates a location of a transition in the values stored in the parallel latch, and wherein the weighted encoder outputs a weighted numerical value that corresponds to the transition location signal; and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HLN
November 09, 2006

TIMOTHY P. CALLAHAN
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